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10/059,727	01/29/2002	Luan Tran	MCT.0004C1US	7665

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EXAMINER	
FENTY, JESSE A	

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.

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Commissioner for Patents

Attached please find a copy of the Examiner's Answer sent 03/09/04. Conferees' signatures have been added for the record.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 12

Application Number: 10/059,727
Filing Date: January 29, 2002
Appellant(s): TRAN ET AL.

Dan C. Hu, Reg. No. 40,025
For Appellant

EXAMINER'S ANSWER

This is in response to the Appeal Brief filed Nov. 18, 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct; however, claim 9 has not been re-written in independent form as asserted by Applicant.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The appellant's statement in the brief that certain claims do not stand or fall together is not agreed with because objected to claim 9 is included in Group 2. Therefore, Group 2 only includes claims 6-8, 10 and 16.

(8) Claims Appealed

A substantially correct copy of appealed claims 1-25 appears on pages i-iv of the Appendix to the appellant's brief. The minor errors are as follows: previously objected to claim 9, overcome by a Terminal Disclaimer, has not been rewritten in independent form. Therefore, claim 9 is allowable.

(9) Prior Art of Record

5,747,844	Aoki et al.	05-1995
5,107,459	Chu et al.	04-1992

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 and 10-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. Patent No. 5,747,844) in view of Chu et al. (U.S. Patent No. 5,107,459).

In re claims 1, 10-12, and 17-19, Aoki (Fig. 6) discloses a semiconductor device, comprising:

Memory cells each having an area of about $6F^2$;

Sense amplifiers;

Active area lines (2), transistors being formed in the active area lines and electrically coupling corresponding memory cells to corresponding first level bit lines; and

Bit lines (BL1, BL2, ..) coupled to the sense amplifiers in a folded and open bit line configurations (Background of the Invention). Aoki does not expressly disclose the folded bit line configuration reaching the $6F^2$ dimension, though Aoki does recognize the development of semiconductor technology on an ever-decreasing size scale. Dimensions for folded bit lines of the $6F^2$ size were known in the art at the time of the invention (as disclosed by Teaching reference Keeth et al. (US 2003/0071295) cited in Final Office Action mailed 06/18/03)). It would have been obvious for one skilled in the art at the time of the invention to scale a folded bit line to a smaller size for the purpose, for example, of enhancing the integration density of the MOS device (Aoki; column 1, lines 17-22).

Aoki discloses each bit line including a first level portion and a second level portion, but does not express disclose each bit line being on a separate (vertical) level. Chu discloses bit lines (BL1 and BL2) vertically separated from one level to another in a folded bit-line array. It would have been obvious to one skilled in the art at the time of the invention to configure the device of Aoki in the manner disclosed by Chu for the purpose, for example of achieving a higher density memory cell architecture (Chu; Abstract.)

In re claims 2, 13 and 20, Aoki in view of Chu discloses the devices of claims 1, 11 and 19 respectively, wherein each pair of bit lines is vertically twisted at one or more predetermined

locations, the bit liens in the pair transitioning between the first level portion and the second level portion at each twist.

In re claim 3, Aoki in view of Chu discloses the device of claim 2, wherein a column pitch of each memory cell is 2F.

In re claims 4, 14 and 21, Aoki in view of Chu discloses the devices of claims 1, 12 and 20 respectively, wherein each memory cell includes a capacitor formed over the first level portion of each bit line.

In re claims 5, 15 and 22, Aoki in view of Chu discloses the devices of claims 4, 14 and 21, wherein the second level portion of each bit line is formed over each capacitor.

In re claims 6, and 16, Aoki in view of Chu discloses the devices of claims 1 and 11 respectively, wherein the bit lines extend generally along the same direction as the active area lines, the bit lines intersecting the active area lines at slanted portions.

In re claim 7, Aoki in view of Chu discloses the device of claim 6, wherein the active area lines are generally straight and the bit lines extend in a wavy pattern.

In re claim 8, Aoki in view of Chu discloses the device of claim 6, wherein the bit lines are generally straight and the active area lines extend in a wavy pattern.

In re claim 10, Aoki in view of Chu discloses the device of claim 6, wherein the bit lines extend along generally the same direction as the active area lines so that the bit lines and active area lines intersect at predetermined locations.

In re claims 23, 24 and 25, Aoki in view of Chu discloses the devices of claims 1, 11 and 18 respectively, wherein in the folded bit line arrangement a pair of bit liens is coupled to a same side of each corresponding sense amplifier.

(11) Response to Argument

A. Are claims 1-5, 11-15, 17, 18 and 20-25 obvious over the asserted combination of Aoki and Chu?

Applicant quotes the MPEP regarding the basic requirement for a *prima facie* case of obviousness that the prior art *must* suggest the desirability of the claimed invention. This requirement is met by the principal reference, Aoki, which discloses the desirability of shrinking the device size of a semiconductor component to enhance the integration density (Aoki; column 1, lines 17-22).

The main issue in this application is one of the dimensions and/or scaling of Folded Bit Line memory structures. Applicant first argues that the device disclosed by Aoki teaches away from the use of the Folded Bit Line architecture size ($8F^2$), by using the smaller Open Bit Line architecture size ($6F^2$). Aoki teaches away from a Folded Bit Line structure because the smallest dimension known to Aoki at the time for a Folded Bit Line configuration was $8F^2$. However, a reference that teaches away from a device feature does not make use of that feature fatal. MPEP § 2145(X)(D)(1) states that, "[A] known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." Aoki discolses the shortcomings of both the Open and Folded Bit Line architectures (Background of the Invention), but uses the Open architecture because of the smaller size.

The size dimension in this application cannot be considered the sole determining factor for patentability. Additional references have been cited, e.g. Keeth et al. (U.S. 2003/0071295), that demonstrate the claimed dimension was known to the prior art at the time of filing.

Additionally, the MPEP has addressed the issue of size dimensions in § 2144.04 regarding Changes in Size/Proportion in several cases including:

In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955) (Claims directed to a lumber package "of appreciable size and weight requiring handling by a lift truck" where held unpatentable over prior art lumber packages which could be lifted by hand because limitations relating to the size of the package were not sufficient to patentably distinguish over the prior art.); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976) ("mere scaling up of a prior art process capable of being scaled up, if such were the case, would not establish patentability in a claim to an old process so scaled." 531 F.2d at 1053, 189 USPQ at 148.); and in *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

There is no argument that the claimed $6F^2$ device will function in a different manner than the $8F^2$ device of Aoki, the only issue is the obviousness of the size differential. The Folded Bit Line $6F^2$ dimension, shown to be a desirous dimension by Aoki, was known in the art at the time of the instant application was filed (Mori, '784, column 4, lines 47-51). As stated by Keeth, '307 (column 1, lines 26-35), "Manufacturing of these chips, at first, was not concerned with shrinking every part down to its smallest size... However, once the DRAMS reached the 256K-memory density, shrinking of all features became important." Obtaining smaller device sizes in

a constant innovation in the semiconductor industry, as noted by Aoki. The smaller device dimension in this instance should not be the determining factor in granting patentability.

B. Are Claims 6-8, 10 and 16 obvious over the asserted combination of Aoki and Chu?

Applicant argues that Aoki in view of Chu does not disclose the claimed elements of bit lines coupled to sense amplifiers in a folded bit line configuration; and bit lines intersecting active area lines and slanted portions, with contacts formed in the slanted portions.

The folded bit line configuration is addressed in Part A of the Argument. Figure 6 of Aoki discloses active area lines (2), bit lines (BL1, BL2, ...) and contact areas (1). The active area lines have small slanted portions that intersect the bit line, as well as horizontal portions that lay above, below and collinear with the bit lines. However, taking all of the portions of the active area line together, the entire active area line is slanted; and in the middle of this active area line, the contact (1) is formed. Thus, the cited prior art reads on the claims.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Jesse A. Fenty
Examiner
Art Unit 2815

November 26, 2004

Appeal Conference held on January 17, 2004 with:

SPE Olik Chauhuri
SPE Tom Thomas T. T.

Tom Thomas

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